REMARKS

The present Amendment cancels claim 1, amends claims 2-14, and adds claim 15. Therefore, the present application has pending claims 2-15.

Request for Correction of Patent Office Records

Applicants filed the present application on February 27, 2002. The Patent and Trademark Office mailed a Notice to File Missing Parts – Filing Date Granted on April 4, 2002. Applicants filed a Submission of Verified English Translation of Specification on April 17, 2002. Thereafter, all of the Patent Office communications reflected an April 17, 2002 filing date for the application. Applicants respectfully request that the Patent Office records be corrected to show the original filing date of February 27, 2002.

35 U.S.C. §103 Rejections

Claims 1-3, 7, 10, and 12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,999,415 to Luijten, et al. ("Luijten") in view of *Design and Implementation of Abacus Switch: A Scalable Multicast ATM Switch, Selected Areas in Communications*, IEEE Journal, Vol. 15, Issue 5, June 1997, p. 830-843 by Chao, et al. ("Chao"). As discussed above, claim 1 was canceled. Therefore, this rejection with respect to claim 1 is rendered moot.

With regard to claims 2, 3, 7, and 10, this rejection is traversed for the following reasons. Applicants submit that claims 2, 3, 7, and 10, as now more clearly recited, are dependent on new claim 15. Therefore, claims 2, 3, 7, and 10 are

allowable for at least the same reasons provided regarding independent claim 15, as discussed below.

With regard to the remaining claim 12, Applicants traverse this rejection for the following reasons. Applicants submit that the features of the present invention, as now more clearly recited in claim 12, are not taught or suggested by either Luijten or Chao, whether taken individually or in combination with each other in the manner suggested by the Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Amendments were made to the claims to more clearly describe features of the present invention. Specifically, amendments were made to more clearly describe that the present invention is directed to a packet data transfer controlling method as recited, for example, in independent claim 12.

The present invention, as recited in claim 12, provides a packet data transfer controlling method. The method includes a step of storing, by each of a plurality of ingress interfaces, packet data received from an input line in one of a plurality first storing unit, and shifting a first data portion including destination information of the packet data from the first storing unit to one of a plurality of second storing units, which is paired with the first storing unit. The method also includes a step of controlling, by control units, one of the second storing units, so as to transfer the first data portion to one of the third storing units, leaving the same data in the second storing unit. Another step includes selecting, by a scheduler, at least one of the third storing units that stores the first data portion allowed to be transferred to one of the

output ports. The method also includes controlling, by each of the control units, in response to a predetermined control signal from the scheduler, one of the first storing units, which is paired with the second storing unit from which the first data portion has been transferred, so as to transfer a remaining portion of the packet data to one of the third storing units selected by the scheduler. Yet another step of the method includes transferring, by the switch unit, the first data portion and remaining portion output from the selected third storing unit to one of the output ports specified by the destination information of the first data portion. The method also includes controlling, by each of the control units that could not receive the predetermined control signal, another of the second storing units so as to transfer the first data portion to one of the third storing units, thereby replacing the previous first data portion with the new first data portion in the third storing unit. The prior art does not teach all of these features.

The above described features of the present invention, as now more clearly recited in claim 12, are not taught or suggested by any of the references of record. Specifically, the features are not taught or suggested by either Luijten or Chao, whether taken individually or in combination with each other.

Luijten is directed to a switching device and method for controlling the routing of data packets. However, there is no teaching or suggestion in Luijten of the packet data transfer controlling method as recited in claim 12.

Luijten's switching device includes several input ports and several output ports, where each of the input ports is connectable to a corresponding switch

adapter. At least one switch controller controls the routing of incoming data packets from the input ports to the output ports. For each output port, a congestion controller is arranged. In operation, the congestion controller generates grant information, which signals whether the switch adapters are allowed to send the data packet to the output port. For each of the input ports, a data packet access controller marks a data packet as non-compliant if the packet was erroneously sent from the output port.

One step of the present invention, as recited in claim 12, includes storing, by each of a plurality of ingress interfaces, packet data received from an input line in one of a plurality of first storing units, and shifting a first data portion including destination information of the packet data from the first storing unit to one of a plurality of second storing units, which is paired with the first storing unit. Luijten does not disclose this step. To support the assertion that Luijten discloses storing packet data in a first storing unit and transferring a data portion including destination information of packet data to a second storing unit, the Examiner cites column 4, lines 20-21, which states, "the arriving data packets are sorted in each input buffer 11 according to their destination output port 30". However, this is quite different from the step of storing packet data, as claimed. More specifically, neither the cited text nor any other portions of Luijten teach or suggest storing, by each of a plurality of ingress interfaces, packet data received from an input line in one of a plurality of first storing units, and shifting a first data portion including destination information of the

packet data from the first storing unit to one of a plurality of second storing units paired with the first storing unit, as claimed.

Another step of the present invention, as recited in claim 12, includes controlling, by each of the control units that could not receive the predetermined control signal, another of the second storing units so as to transfer the first data portion to one of the third storing units, thereby replacing the previous first data portion with the new first data portion in the third storing unit. Luijten does not disclose this step.

Therefore, Luijten fails to teach or suggest "storing, by each of said ingress interfaces, packet data received from said input line in one of said first storing units, selectively and shifting a first data portion including destination information of the packet data from the first storing unit to one of said second storing units, which is paired with the first storing unit" as recited in claim12.

Furthermore, Luijten fails to teach or suggest "controlling, by each of said control units that could not receive said predetermined control signal, another of said second storing units so as to transfer the first data portion to one of said third storing units, thereby to replace the previous first data portion with the new first data portion in the third storing unit" as recited in claim 12.

The above noted deficiencies of Luijten are not supplied by any of the other references, particularly Chao. Therefore, combining the teachings of Chao with Luijten still fails to teach or suggest the features of the present invention, as now more clearly recited in the claims.

Chao discloses the design and implementation of an abacus switch, or more specifically, a scalable multicast asynchronous transfer mode (ATM) switch. However, there is no teaching or suggestion in Chao of the packet data transfer controlling method as recited in claim 12.

Chao's multicast ATM switch is scalable from a few tens to a few thousands of input ports. The switch, which is called an abacus switch, has a non-blocking switch fabric followed by small switch modules at the output ports. It has buffers at the input and output ports. Cell replication, cell routing, output contention and resolution, and cell addressing are all performed in a distributed way so that it can be scaled up to thousands of input and output ports.

One step of the present invention, as recited in claim 12, includes storing, by each of a plurality of ingress interfaces, packet data received from an input line in one of a plurality of first storing units, and shifting a first data portion including destination information of the packet data from the first storing unit to one of a plurality of second string units, which is paired within the first storing unit. Chao does not disclose this step, and the Examiner has not relied upon Chao for teaching a step of storing packet data in the manner claimed.

Another step of the present invention, as recited in claim 12, includes controlling, by each of the control units that could not receive the predetermined control signal, another of the second storing units so as to transfer the first data portion to one of the third storing units, thereby replacing the previous first data portion with the new first data portion in the third storing unit. Chao does not

disclose this step. For example, as indicated in the third paragraph on page 836, Chaos discloses a mechanism for retransmitting a cell in a stack state. This feature is quite different from controlling another of the second storage units, as claimed.

Therefore, Chao fails to teach or suggest "storing, by each of said ingress interfaces, packet data received from said input line in one of said first storing units, selectively and shifting a first data portion including destination information of the packet data from the first storing unit to one of said second storing units, which is paired with the first storing unit" as recited in claim12.

Furthermore, Chao fails to teach or suggest "controlling, by each of said control units that could not receive said predetermined control signal, another of said second storing units so as to transfer the first data portion to one of said third storing units, thereby to replace the previous first data portion with the new first data portion in the third storing unit" as recited in claim 12.

Both Luijten and Chao suffer from the same deficiencies relative to the features of the present invention, as recited in claim 12. Therefore, combining the teachings of Luijten and Chao, in the manner suggested by the Examiner, does not render obvious the features of the present invention, as now more clearly recited in claim 12. Accordingly, reconsideration and withdrawal of the 35 U.S.C. §103(a) rejection of claim 12 as being unpatentable over Luijten in view of Chao are respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references used in the rejection of claim 12.

Claim 4 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Luijten in view of Chao, and further in view of U.S. Patent No. 5,140,582 to Tsuboi, et al. ("Tsuboi"). This rejection is traversed for the following reasons. Applicants submit that claim 4, as now more clearly recited, is dependent on new claim 15. Therefore, claim 4 is allowable for at least the same reasons provided regarding independent claim 15, as discussed below.

New Claim 15

Claim 15 was added to more clearly describe features of the present invention. Specifically, claim 15 was added to more clearly describe that the present invention is directed to a packet communication apparatus.

The present invention, as described in claim 15, provides a packet communication apparatus, which includes a switch unit, a plurality of ingress interfaces, and a plurality of egress interfaces. The switch unit includes a scheduler for scheduling packet transfer between a plurality of input ports and a plurality of output ports, and further includes a plurality of ingress buffers, each connected to one of the input ports. The ingress interfaces are each connected to one of the ingress buffers and selectively transfers packets received from an input line to the ingress buffer. The egress interfaces are each connected to one of the output ports,

and transmits packets received from the switch unit to an output line. In the apparatus of the present invention, each of the ingress interfaces includes plural pairs of queue buffers for storing packet data and a register configured to retransmit stored packet data, and further includes a buffer control unit for selecting one of the pairs of queue buffers to output stored packet data. The register of the selected pair stores a first data block including header information of a packet received from one of the input lines and routing information for specifying one of the output ports. The queue buffer of the selected pair stores the remaining portion of the received packet. Also in the present apparatus of the present invention, said buffer control unit controls the selected register to output the first data block to one of the ingress buffers. In addition, the scheduler issues an acknowledge signal to the buffer control unit if a path toward the output port specified with the routing information of the first data block in the ingress buffer is available to the ingress buffer. The present invention also includes where the buffer control unit controls the selected queue buffer to output the remaining portion of the received packet to the ingress buffer after receiving the acknowledge signal. Otherwise, the buffer control unit selects one of the other pairs of queue buffer and register to output a new first data block from the register to one of the ingress buffers, thereby replacing the previous first data block with the new first data block in the ingress buffer. The prior art does not disclose all these features.

The above described features of the present invention, as recited in claim 15, are not taught or suggested by any of the references of record. Specifically, the

features are not taught or suggested by either Luijten or Chao, whether taken individually or in combination with each other.

As previously discussed, Luijten is directed to a switching device and method for controlling the routing of data packets. However, there is no teaching or suggestion in Luijten of the packet communication apparatus as recited in claim 15.

Features of the present invention, as recited in claim 15, include where each of the ingress interfaces has plural pairs of queue buffers that store packet data, a register that can retransmit stored packet data, and a buffer control unit for selecting one of the pairs of queue buffers to output stored packet data. The register of the selected pair of queue buffers stores a first data block including header information of a packet received from one of the input lines and routing information for specifying one of the output ports. The queue buffer of the selected pair stores the remaining portion of the received packet. Luijten does not disclose each of these features.

For example, Luijten does not teach or suggest where each of the ingress interfaces includes a buffer control unit, as claimed. In the rejection of claim 1 (now canceled), the Examiner asserts that the data packet access controller 40, which is connected to each input port 20 within a switching device 10, corresponds to the scheduler of the present invention. Furthermore, the Examiner asserts that the control unit 25 corresponds to the buffer control unit of the present invention. However, as described in paragraph 4, lines 30-62, the purpose of the control unit 25 is to lead the data packets that arrive via adapter input lines 50 to output ports 30. the control unit 25 provides the necessary connections between the input ports 20

and the output ports 30, according to the data packet destination information that is contained in each data packet header, and signals to the input buffers 11 when the path for the next data packet in the respective input buffer 11 is free, such that this data packet can be taken from the input buffer 11 and sent to its destination. Based on this description, it is apparent that the control unit 25 corresponds to the scheduler of the present invention, and that Luijten fails to disclose a plurality of buffer control units, where each of the ingress interfaces includes a buffer control unit, in the manner claimed.

Other features of the present invention, as recited in claim 15, include where the scheduler issues an acknowledge signal to the buffer control unit if a path toward the output port specified with the routing information of the first data block in the ingress buffer is available to the ingress buffer. Luijten does not disclose this feature.

Additional features of the present invention, as recited in claim 15, include where the buffer control unit controls the selected queue buffer to output the remaining portion of the received packet to the ingress buffer after receiving the acknowledge signal. Otherwise, the buffer control unit selects one of the other pairs of queue buffer and register to output a new first data block from the register to one of the ingress buffers to replace the previous first data block with the new first data block in the ingress buffer. This feature is not disclosed in Luijten.

Therefore, Luijten fails to teach or suggest "wherein each of said ingress interfaces has plural pairs of queue buffers for storing packet data and a register

capable of retransmitting stored packet data, and a buffer control unit for selecting one of said pairs of queue buffers to output stored packet data, the register of the selected pair storing a first data block including header information of a packet received from one of said input lines and routing information for specifying one of said output ports, the queue buffer of the selected pair storing the remaining portion of the received packet" as recited in claim15.

Furthermore, Luijten fails to teach or suggest "wherein said scheduler issues an acknowledge signal to the buffer control unit if a path toward the output port specified with the routing information of the first data block in the ingress buffer is available to the ingress buffer" as recited in claim 15.

Even further, Luijten fails to teach or suggest "wherein the buffer control unit controls the selected queue buffer to output the remaining portion of the received packet to the ingress buffer after receiving said acknowledge signal, and otherwise, the buffer control unit selects one of the other pairs of queue buffer and register to output a new first data block from the register to one of said ingress buffers, thereby to replace the previous first data block with the new first data block in the ingress buffer" as recited in claim 15.

The above noted deficiencies of Luijten are not supplied by any of the other references, particularly Chao. Therefore, combining the teachings of Chao with Luijten still fails to teach or suggest the features of the present invention, as now more clearly recited in the claims.

As previously discussed, Chao discloses the design and implementation of an abacus switch, or more specifically, a scalable multicast asynchronous transfer mode (ATM) switch. However, there is no teaching or suggestion in Chao of the packet data transfer controlling method as recited in claim 15.

Features of the present invention, as recited in claim 15, include where each of the ingress interfaces has plural pairs of queue buffers that store packet data, a register that can retransmit stored packet data, and a buffer control unit for selecting one of the pairs of queue buffers to output stored packet data. The register of the selected pair of queue buffers stores a first data block including header information of a packet received from one of the input lines and routing information for specifying one of the output ports. The queue buffer of the selected pair stores the remaining portion of the received packet. Chao does not disclose these features. For example, as indicated in the third paragraph on page 836, Chao discloses a mechanism for retransmitting a cell in a stack state. This feature is quite different from storing packet data and a register capable of retransmission, as claimed.

Other features of the present invention, as recited in claim 15, include where the scheduler issues an acknowledge signal to the buffer control unit if a path toward the output port specified with the routing information of the first data block in the ingress buffer is available to the ingress buffer. Chao does not disclose this feature.

Additional features of the present invention, as recited in claim 15, include where the buffer control unit controls the selected queue buffer to output the remaining portion of the received packet to the ingress buffer after receiving the

acknowledge signal. Otherwise, the buffer control unit selects one of the other pairs of queue buffer and register to output a new first data block from the register to one of the ingress buffers to replace the previous first data block with the new first data block in the ingress buffer. Chao does not disclose this feature.

Therefore, Chao fails to teach or suggest "wherein each of said ingress interfaces has plural pairs of queue buffers for storing packet data and a register capable of retransmitting stored packet data, and a buffer control unit for selecting one of said pairs of queue buffers to output stored packet data, the register of the selected pair storing a first data block including header information of a packet received from one of said input lines and routing information for specifying one of said output ports, the queue buffer of the selected pair storing the remaining portion of the received packet" as recited in claim15.

Furthermore, Chao fails to teach or suggest "wherein said scheduler issues an acknowledge signal to the buffer control unit if a path toward the output port specified with the routing information of the first data block in the ingress buffer is available to the ingress buffer" as recited in claim 15.

Even further, Chao fails to teach or suggest "wherein the buffer control unit controls the selected queue buffer to output the remaining portion of the received packet to the ingress buffer after receiving said acknowledge signal, and otherwise, the buffer control unit selects one of the other pairs of queue buffer and register to output a new first data block from the register to one of said ingress buffers, thereby

to replace the previous first data block with the new first data block in the ingress buffer" as recited in claim 15.

Both Luijten and Chao suffer from the same deficiencies relative to the features of the present invention, as recited in claim 15. Therefore, combining the teachings of Luijten and Chao does not render obvious the features of the present invention, as recited in claim 15. Accordingly, reconsideration and withdrawal of the 35 U.S.C. §103(a) rejection of claim 15 as being unpatentable over Luijten in view of Chao are respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references used in the rejection of claim 15.

In view of the foregoing amendments and remarks, Applicants submit that claims 2-15 are in condition for allowance. Accordingly, early allowance of such claims is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the

eposit account of Mattingly, Stanger, Malur & Brundidge, P.C., Deposit Account No. 50-1417 (referencing attorney docket no. 520.41245X00).

Respectfully submitted,

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